## REMARKS

By this Amendment, Applicants amend claims 29 and 35-37, cancel claims 30 and 33, and add new claims 38 and 39.

Accordingly, claims 29 and 34-39 remain pending in the application.

## 35 U.S.C. § 103

The Office Action rejects claims 29 and 34-37 under 35 U.S.C. § 103 over Bollinger et al. U.S. Patent 5,200,358 ("Bollinger") in view of Pfiester U.S. Patent 5,024,959 ("Pfiester").

Applicants respectfully submit that all of the pending claims are patentable over the cited prior art for at least the following reasons.

Among other things, the device of claim 29 includes an etch stop layer formed on the substrate, including on the gate electrode.

The Office Action fairly admits that Bollinger does not disclose such an etch stop layer. However, the Office Action states that Pfiester discloses an etch stop layer 26, and that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bollinger's semiconductor device with the etch stop layer as taught by Pfiester "to minimize the number of lithography masking steps," citing col. 1, lines 15-18 of Pfiester.

Applicants respectfully disagree.

There is absolutely **nothing** at all in the cited text of Pfiester that even remotely suggests that Pfiester's etch stop layer 26 has anything at all to do with minimizing a number of lithography masking steps. Indeed, it is difficult to image how the addition of an additional etch stop layer to Bollinger could possibly reduce the number of lithography masking steps in the process of making Bollinger's device.

Furthermore, Bollinger already teaches that the layers 15 and 17 should have different etch rates so that layer 15 can function as an etch stop when layer 17 is etched (col. 3, lines 9-11, 26-31 and see FIG. 3). What is the point then of adding another etch stop layer, and where is the motivation to do so?

Finally, claim 1 does not merely recite the presence of "an etch stop layer." Instead, it very clearly describes a structural relationship where the etch stop layer is formed on the substrate including the gate electrode, and the undoped and doped insulating layers are formed in turn on the etch stop layer. The Office Action does not provide any explanation as to how or why one would have supposedly been motivated to modify Bollinger to add an etch stop layer that would be beneath both insulating layers 15 and 17. Indeed, this would seem to make no sense as it is very clear from inspection of FIGs. 3-6 of Bollinger that Bollinger intends for insulating layer 15 to remain on the gate electrodes and between the gate electrodes, and not to be etched through. In that case, an etch stop layer added beneath insulating layer 15 makes no sense at all.

Therefore, Applicants traverse the proposed combination of Bollinger and Pfiester as lacking any motivation in the prior art.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 29 is patentable over the cited prior art.

Claims 34, 35 and 37

Claims 34, 35 and 37 depend from claim 29 and are deemed patentable for at least the reasons set forth above with respect to claim 29.

Claim 36

Claim 36 has been amended to be in independent form, and to eliminate the process features which the Examiner has declined to accord patentable weight.

Among other things, in the device of claim 36, the doped insulating layer contains about 5.5% by weight of boron and about 3.0% weight of phosphorus.

The Office Action does not even allege that any of the cited references disclose such features, but instead states that Applicants must show that the "chosen dimensions" are critical.

At the outset, the above-recited features of claim 36 are not "dimensions." Instead, claim 36 recites unique and beneficial percentages of elements boron and phosphorous in the doped insulating layer. Such percentages are apparently neither

disclosed or suggested by any of the cited references. Moreover, surely the Examiner has noted the repeated statements throughout Applicants' specification attesting to the benefit of these ratios. For example, paragraph [0120] of the specification explains that when the amount of boron and phosphorous is not controlled, as is the case in prior art devices, the reliability of the semiconductor device fabricating method is reduced. However, as taught in the present specification, by controlling the process gases to produce a doped insulating layer that contains about 5.5% by weight of boron and about 3.0% weight of phosphorus, then BPSG layer flows sufficiently into and fills the recess regions between gate electrodes (see paragraph [0755]; see also, paragraphs [0095]; [0115]; [0395]-[0400]; [0470]-[0475]; [0545]-[0550]; and [0750]).

Therefore, the recited composition of the doped insulating layer is not arbitrary, but instead is carefully selected to provide unique benefits which are clearly identified in the specification. The prior art not disclosing or suggesting a device such as that of claim 36 including a doped insulating layer of the recited composition, Applicants respectfully submit that the device of claim 36 is patentable over the prior art.

Also among other things, the device of claim 36 includes an etch stop layer disposed on the substrate, including on the gate electrode.

As explained above with respect to claim 29, Applicants respectfully submit that no proper combination of cited references would produce a device including this feature in combination with the other features of claim 36.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 36 is patentable over the cited prior art.

## CLAIMS 38-39

Claims 38 and 39 depend respectively from claims 29 and 36, and are each deemed patentable for at least the reasons set forth above with respect to claims 29 and 36, respectively, and for the following additional reasons.

Among other things, each of the devices of claims 38-39 includes a second gate electrode, where the doped insulating layer has a hole formed therein between the first

and second gate electrodes, and wherein sidewalls of the hole comprise the doped insulating layer such that the hole is separated and spaced apart from the first and second gate electrodes.

None of the prior art references discloses such an arrangement of features.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claims 38-39 are patentable over the cited prior art.

## CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 29 and 34-39, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283-0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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